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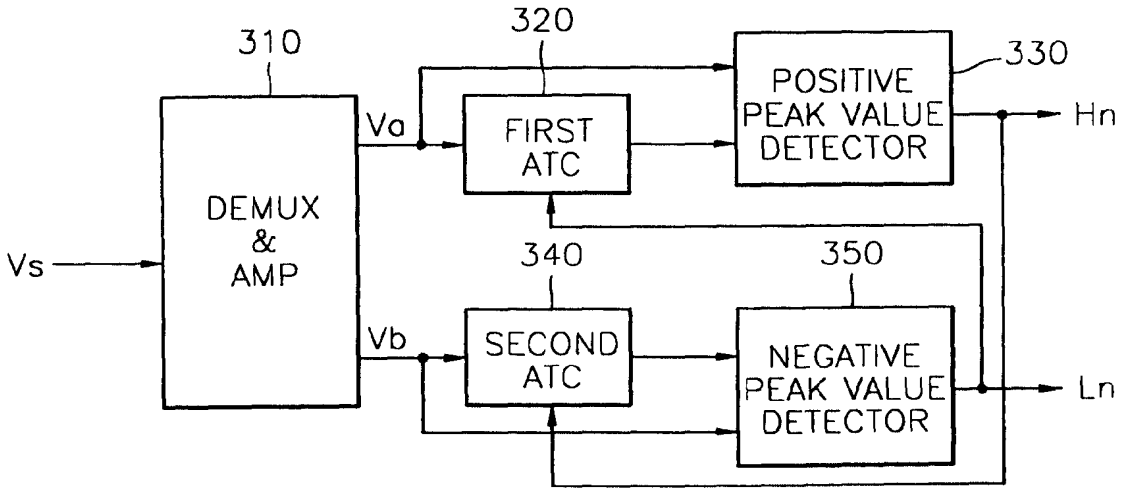
(54) Peak detector using automatic threshold control and method therefor

(57) A peak detector (304) for a maximum likelihood decoding system (303), using an automatic threshold control (ATC), and a method therefor are provided. In the peak detector, positive and negative peak values are detected (330, 350) from an input signal having digital information, based on positive and negative threshold values, and then each threshold value is detected (320, 340) according to positive and negative values of the input signal, to reset each threshold value to a predetermined value based on the detected peak value having the opposite polarity thereto. Accordingly, data can be detected exactly, improving performance of Viterbi decoding.

FIG. 6



EP 0 889 590 A1

Description

The present invention relates to in general to the field of maximum likelihood decoding, and more particularly, to an apparatus for improving performance of Viterbi decoding by effectively detecting the peak value of an input signal using automatic threshold control (ATC) for detecting digital information of an input signal, and a method therefor.

For increasing the recording density of a signal without a significant change in the characteristics of the conventional recording/reproducing system, technology relating to partial response maximum likelihood (PRML), including a Viterbi decoding process, has been advanced, and a lot of specific circuits have been suggested.

Figure 1 is a block diagram of a digital recording/reproducing apparatus as an example of the PRML-4 system. In Figure 1, analog video and audio signals are converted into digital data by first and second analog-to-digital (A/D) converters 110 and 120. The video data output from the first A/D converter 110 is compressed through a high-efficiency coding process by a video data encoder 130, and then output to an error correction encoder 150. The audio data output from the second A/D converter 120 is coded by an audio data encoder 140 to be suitable for recording, and then also output to the error correction encoder 150. The error correction encoder 150 mixes the video data output from the video data encoder 130 and the audio data output from the audio data encoder 140, and adds a parity to the data using an error correction code, e.g., Reed Solomon code, to output the error-correction-coded data to a recording encoder 160. The recording encoder 160 modulates the error-correction-coded data according to a predetermined modulation scheme to be suitable for the characteristics of a recording channel, equalizes the modulated data to compensate for nonlinearities in the recording process, and outputs the equalized result to a recording amplifier 170. The signal amplified by the recording amplifier 170 is recorded on a recording medium T by a recording head HD1.

The signal recorded on the recording medium T is reproduced by a playback head HD2, and then amplified by a playback amplifier 210. A data detector 220 detects video and audio data from the amplified signal. An error correction decoder 230 corrects errors in the video and audio data detected by the data detector 220, and outputs the error-correction-decoded video and audio data to a video data decoder 240 and an audio data decoder 250, respectively. The video data decoder 240 decodes the error-correction-decoded video data to output video data to be finally restored by a first digital-to-analog (D/A) converter 260. The audio data decoder 250 decodes the error-correction-decoded audio data to output audio data to be finally restored by the second D/A converter 270.

Figure 2 is a detailed block diagram of the data detector shown in Figure 1, for detecting the data by a digital method. In Figure 2, an automatic gain control (AGC) amplifier 221 automatically controls the amplitude of a reproduced signal amplified by the playback amplifier 210 of Figure 1 to have a constant level. A low-pass filter (LPF) 222 low-pass-filters the signal output from the AGC amplifier 221 to remove a high frequency component of noise overlapping with the signal in the output of the AGC amplifier 221. An A/D converter 223 converts the low-pass filtered signal into digital data, and an equalizer 224 compensates distortion in the waveform and amplitude of the digital data to output the result to a maximum likelihood decoder 225. A timing detector 226 detects the timing of the reproduced signal equalized by the equalizer 224 using a phase-locked loop (PLL) included therein, and outputs a driving clock which is required for the A/D converter 223, the equalizer 224 and the maximum likelihood decoder 225. A channel demodulator 227 demodulates the maximum-likelihood-decoded data output from the maximum likelihood decoder 225 based on a modulation scheme used for the modulation, and outputs the result to the error correction decoder 230 of Figure 1.

Here, the maximum likelihood decoder 225 includes a Viterbi decoder for determining whether data detected at a given time is precise, or data which passed through a trellis diagram is correct. That is, the Viterbi decoder calculates metrics for each pass to select a surviving path, and stores information of the surviving pass in a memory according to each state, thereby decoding the input data by the final surviving path data read out from the memory, having the same shape as the trellis diagram.

Also, a peak detector using a conventional automatic threshold control (ATC) is installed before the Viterbi decoder of the maximum likelihood decoder 225. When the states are binary, a peak value of the signal in the positive direction (hereinafter, "positive peak") and a peak value of the signal in the negative direction (hereinafter, "negative peak") basically correspond to the metrics. Thus, the peak detector enables the detection of the positive peak of the input signal for maintaining the level of that value as a new threshold to detect consecutive positive peaks, and for updating a threshold for detecting the negative peak. Here, in the same manner, the peak detector enables the detection of the negative peak of the input signal for maintaining the level of that value as a new threshold to detect consecutive negative peaks and for updating a threshold for detecting the positive peak.

An example of the above-mentioned peak detector is shown in Figure 3. In Figure 3, a positive peak value detector 225.2 with a comparator COMP1, and a negative peak value detector 225.3 with a comparator COMP2, simultaneously detect positive and negative peak values of the equalized signal output via an amplifier 225.1. That is, the positive and negative peak values of the output signal from the equalizer 224 of Figure 2

are detected while maintaining an offset A which is a predetermined difference between threshold values T_H and T_L of the positive peak value detector 225.2 and the negative peak detector 225.3. Here, the offset A is equal to Vr+Vd, and updating the threshold values according to the input signal and maintaining the difference between the threshold values of the positive peak value detector 225.2 and the negative peak detector 225.3 with a constant offset is called "ATC".

The operation principle of the peak detector of Figure 3 is shown in Figure 4. That is, the positive peak value detector 225.2 has an output Hn of logic "1" when an input signal Vi output from the amplifier 225.1 is greater than the threshold value T_H for the positive peak value detection (hereinafter simply referred to as "positive threshold value"), and of logic "0" otherwise. The negative peak value detector 225.3 has an output Ln of logic "1" when the input signal Vi is less than the threshold value T_L for the negative peak value detection (hereinafter simply referred to as "negative threshold value"), and of logic "0" if otherwise.

As described above, if the positive peak value is detected, the detected value is maintained to be set as a new positive threshold value, and simultaneously the negative threshold value is updated to a value which is less than the positive threshold value by the offset A. Updating the negative threshold value to be less than the positive threshold by the offset A is because the minimum distance of the metrics is determined when the negative peak value is detected following the positive peak value. In addition, a path of the trellis diagram is decided till a time point at which the previous positive peak value which is the nearest from the detected negative peak value was generated. That is, the path having the minimum metric is selected.

In the same manner, if the negative peak value is detected, the detected value is maintained to be set as a new negative threshold value, and simultaneously the positive threshold value is updated to a value which is greater than the threshold value by the offset A. The predetermined offset A between the negative and positive threshold values changes according to a peak-to-peak value of the input signal.

However, the peak detector of Figure 3 detects the peak value of the input signal having digital information "+1", as an example, when digital information "+1" and "-1" of the input signal are alternately input, to set a new positive threshold value according to the detected peak value, and simultaneously updates a negative threshold value having an opposite polarity of the detected peak value. At this time, if the next input signal having signal information "-1" is input before the negative threshold value is completely updated, a data is detected by a threshold value which does not have a constant offset A. Thus, if the threshold value of the opposite polarity of the detected peak value is not updated completely at an intended time, a data detection error occurs, lowering performance of the Viterbi decoding. In addition, when the peak detector detects the input signal "0" as "1", the detection error can be corrected by a Viterbi decoder. However, if the input signal "1" is detected as "0", this detection error cannot be corrected by the Viterbi decoder. Thus, the data detection error influences the performance of the Viterbi decoding.

It is an aim of at least preferred embodiments of the present invention to provide a peak detector apparatus and method overcoming at least some of the problems discussed above.

It is a particular preferred aim to provide a peak detection apparatus and method for avoiding the problem of data detection error due to a threshold value not being updated in time, as discussed above.

According to a first aspect of the present invention, there is provided a peak detector comprising; a detector which detects positive and negative peak values from an input signal having digital information, based on positive and negative threshold values; and a threshold controller which detects each threshold value according to positive and negative values of the input signal, to reset each threshold value to a predetermined value based on the detected peak value having the opposite polarity thereto.

Also according to the present invention, there is provided a peak detection method comprising the steps of: (a) detecting positive and negative peak values from an input signal having digital information, based on positive and negative threshold values; and (b) detecting each threshold value according to positive and negative values of the input signal, to reset each threshold value to a predetermined value based on the detected peak value having the opposite polarity thereto.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a general digital recording/reproducing apparatus;

Figure 2 is a detailed block diagram of the data detector of Figure 1;

Figure 3 is a detailed circuit diagram of the peak detector included in the maximum likelihood decoder of Figure 2;

Figure 4 is a diagram illustrating the operating principle of the peak detector of Figure 3;

Figure 5 is a block diagram of a preferred data detector;

Figure 6 is a block diagram of a peak detector of Figure 5 according to a preferred embodiment of the present invention;

Figure 7 is a detailed circuit diagram of the peak detector of Figure 6; and

Figures 8A through 8G are operational waveforms of the peak detector of Figure 7.

A peak detector using automatic threshold control (ATC) and a peak detection method according to a preferred embodiment of the present invention will be described.

Figure 5 shows a data detector which is used in the preferred embodiments of present invention, however, the data detector of Figure 2 may be alternatively applied to the present invention. In Figure 5, an automatic gain control (AGC) amplifier 301 automatically controls a reproduced signal output from a playback amplifier to have a constant amplitude, and outputs it to an equalizer 302. A peak detector 304 of a maximum likelihood decoder 303 detects a positive peak value Hn and a negative peak value Ln according to positive and negative threshold values which are set by the equalized signal provided by the equalizer 302 and controlled by the peak value having the opposite polarity. A Viterbi decoder 305 receives the positive peak value Hn and the negative peak value Ln detected by the peak detector 304 to perform a Viterbi decoding. A timing detector 306 detects the timing of the reproduced signal equalized by the equalizer 302 to output driving clock signals required for the equalizer 302 and the Viterbi decoder 305. A channel demodulator 307 demodulates the Viterbi-decoded data based on the modulation scheme used for modulation to output it to an error correction decoder.

The data detector of Figure 5 adopts an analog mode without using an analog-to-digital (A/D) converter, in contrast to the data detector adopting a digital mode of Figure 2. The Viterbi decoder 305 of Figure 5 which functions without using an A/D converter (hereinafter simply referred to as "analog Viterbi decoder") is constituted of a shift register, and the detailed structure and operation thereof are disclosed in U.S. Patent No. 08/743,915 by the same applicant as that of the present invention. The analog Viterbi decoder has a simpler circuit structure than a conventional Viterbi decoder, thereby minimizing area of an integrated circuit (IC). Accordingly, manufacturing costs and power consumption can be reduced.

According to the peak detector and peak detection method of the present invention, the data detection error caused in the conventional peak detector, when a threshold value is not updated in time, does not occur. Also, even though the peak detector of the present invention is applied to the data detector adopting an analog mode of Figure 5, performance similar to that of the data detector adopting a digital mode of Figure 2 can be achieved.

Figure 6 is a block diagram of the peak detector according to a preferred embodiment of the present invention. In Figure 6, a demultiplexer and amplifier (DEMUX & AMP) 310 detects positive (+) values from the equalized signal Vs output from the equalizer 302 of Figure 5, to output a positive signal Va amplified to a predetermined level to a first automatic threshold controller (ATC) 320 and a positive peak value detector 330, and negative (-) values from the equalized signal Vs to output a negative signal Vb amplified to a predetermined level to a second ATC 340 and a negative peak value detector 350.

The first ATC 320 automatically sets a positive threshold value, according to the amplified positive signal Va output from the DEMUX & AMP 310, and resets the positive threshold value to a predetermined value at a time point when a negative peak value is detected by the negative peak value detector 350. The positive peak value detector 330 compares the positive threshold value set by the first ATC 320 with the amplified positive signal Va, to output a positive peak value Hn corresponding to the amplified positive signal Va, and to simultaneously feed back the positive peak value Hn to the second ATC 340.

The second ATC 340 automatically sets a negative threshold value, according to the amplified negative signal Vb output from the DEMUX & AMP 310, and resets the negative threshold value to a predetermined value at a time point when a positive peak value is detected by the positive peak value detector 330. The negative peak value detector 350 compares the negative threshold value set by the second ATC 340 with the amplified negative signal Vb, to output a negative peak value Ln corresponding to the amplified negative signal Vb, and to simultaneously feed back the negative peak value Ln to the first ATC 320.

Figure 7 is a detailed circuit diagram of the peak detector of Figure 6. In Figure 7, the first amplifier (AMP1) 311 outputs a signal Vs(+) having the positive phase from the input signal, i.e., the equalized signal Vs output from the equalizer, and a signal Vs(-) having the negative phase from the input signal, to a second amplifier (AMP2) 312 and a third amplifier (AMP3) 313, respectively. The AMP2 312 selects only positive values, i.e., values corresponding to the detection point of "+1", from the signal Vs(+) output from the AMP1 311, to amplify the positive values to a predetermined level, and then outputs the amplified positive signal Va to the positive peak value detector 330 constituted of a comparator COMP1. The AMP3 313 selects only negative values, i.e., values corresponding to the detection point of "-1", from the negative signal Vs(-) output from the AMP1 311, to amplify the negative values to a predetermined level, and then outputs the amplified negative signal Vb to the negative peak value detector 350 constituted by a comparator COMP2.

The first ATC 320 includes a first half-wave rectifier having a first diode D1 and a first capacitor C1 which are serially connected, and a first transistor Q1 having a base connected to the output of the negative peak value detector 350 via a first base resistor R1, a collector

connected to the output of the first half-wave rectifier and an emitter connected to a reference voltage source Vr. The second ATC 340 includes a second half-wave rectifier having a second diode D2 and a second capacitor C2 which are serially connected, and a second transistor Q2 having a base connected to the output of the positive peak value detector 330 via a second base resistor R2, a collector connected to the output of the second half-wave rectifier and an emitter connected to the reference voltage source Vr.

The positive peak value detector 330 compares the amplified positive signal Va from the AMP2 312, input to a non-inverting port (+), with a positive threshold value Vra from the first half-wave rectifier of the first ATC 320, input to an inverting port (-) and changed according to the amplified positive signal Va, to output a signal Hn which is logic "high" only when the amplified positive signal Va is greater than the positive threshold value Vra, thereby detecting only a positive peak value.

Meanwhile, the output signal Hn of the positive peak value detector 330 is fed back to the base of the second transistor Q2 of the second ATC 340 to control the negative threshold value Vrb input to the inverting port (-) of the negative peak value detector 350. Here, the second transistor Q2 is turned on at only a time point when the output signal Hn of the positive peak value detector 330 becomes logic "high", such that the negative threshold value Vrb becomes equal to the reference voltage Vr, and then prepares to detect a negative peak value.

In the same manner, the negative peak value detector 350 compares the negative signal Vb which is amplified by the AMP3 313, input to a non-inverting port (+), with a negative threshold value Vrb from the second half-wave rectifier of the second ATC 340, input to an inverting port(-), and changed according to the amplified negative signal Vb, to output a signal Ln which is logic "high" only when the amplified negative signal Vb is less than the negative threshold value Vrb, thereby detecting only a negative peak value. Meanwhile, the output signal Ln of the negative peak value detector 350 is fed back to the base of the first transistor Q1 of the first ATC 330 to control the positive threshold value Vra input to the inverting port(-) of the positive peak value detector 330. Here, the first transistor Q1 is turned on at only a time point when the output signal Ln of the negative peak value detector 350 becomes logic "high", such that the positive threshold value Vra becomes equal to the reference voltage Vr, and then prepares to detect a positive peak value.

Here, the data detection performance can be further increased by appropriately setting the positive threshold value Vra determined by the turn-on voltage of the first diode D1 and capacitance of the first capacitor C1, and the negative threshold value Vrb determined by the turn-on voltage of the second diode D2 and capacitance of the second capacitor C2. Also, the reference voltage Vr is shared by the first ATC 320 and the second ATC 340 to simplify the circuit, however, the reference voltage Vr may be separated.

Figures 8A through 8G are operational waveforms of the peak detector of Figure 7. In detail, Figure 8A is a waveform of the input signal Vs of the AMP1 311, Figure 8B is a waveform of the positive signal Vs(+) extracted from the input signal Vs, and Figure 8C is a waveform of the negative signal Vs(-) extracted from the input signal Vs. Also, Figure 8D is a waveform illustrating the operational principle of the positive peak value detector 330, wherein a solid line represents the output signal Va of the AMP2 312 which is input to the non-inverting port (+) of the comparator COMP1, and a dashed line represents the positive threshold value Vra which is output from the first half-wave rectifier and input to the inverting port (-) of the comparator COMP1. Here, the positive threshold value Vra is reset to the reference voltage Vr when the output signal Ln of the negative peak value detector 350, shown in Figure 8G, becomes logic "high".

Figure 8E is a waveform of the output signal Hn of the positive peak value detector 330, and Figure 8F is a waveform illustrating the operational principle of the negative peak detector 350, wherein a solid line represents the output signal Vb of the AMP3 313 which is input to the non-inverting port (+) of the comparator COMP2, and a dashed line represents the negative threshold value Vrb which is output from the second half-wave rectifier of the second ATC 340 and input to the inverting port (-) of the comparator COMP2. Here, the negative threshold value Vrb is reset to the reference voltage Vr when the output signal Hn of the positive peak detector 330, shown in Figure 8E, becomes logic "high". Lastly, Figure 8G is a waveform of the output signal Ln of the negative peak detector 350.

In the described embodiment of to the present invention, the peak detector of is applied to a data detector adopting analog mode, capable of performing the Viterbi decoding without needing an A/D converter and a computing circuit which are required for a digital Viterbi decoder, in a system having a PRML-4(+1,0,-1) channel, such as a digital recording/reproducing apparatus. Thus, power consumption and manufacturing costs can be reduced at the same time. For this reason, the peak detector is suitable for small and low-power consumption goods, such as a digital video camcorder.

The peak detector sets positive and negative threshold values for respectively according to an input signal and resets each threshold value based on the detected peak value having the opposite polarity thereto, to detect the peak value of the input signal. Accordingly, data detection errors caused by incompletely updating the threshold values within the required time can be improved, as well as the performance of the Viterbi decoding.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and docu-

ments are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A peak detector (304) comprising;

   a detector (330,350) which detects positive and negative peak values from an input signal having digital information, based on positive and negative threshold values; and

   a threshold controller (320,340) which detects each threshold value according to positive and negative values of the input signal, to reset each threshold value to a predetermined value based on the detected peak value having the opposite polarity thereto.

2. A peak detector (304) for a maximum likelihood decoding system (303), comprising:

   a positive peak value detector (330) which compares an input signal having digital information with a positive threshold value, to detect the positive peak value;

   a negative peak value detector (350) which compares the input signal with a negative threshold value, to detect the negative peak value;

   a first automatic threshold controller (320) which detects the positive threshold value according to the positive values of the input signal, and which resets the positive threshold value to a predetermined value based on the negative peak value; and

   a second automatic threshold controller (340) which detects the negative threshold value according to the input signal having a negative value, and which resets the negative threshold value to a predetermined value based on the positive peak value.

3. The peak detector of claim 2, wherein the predetermined value of the first automatic threshold controller (320) and the predetermined value of the second automatic threshold controller (340) are the same as each other.

4. The peak detector of claim 2 or 3, wherein the first automatic threshold controller (320) comprises:

   a first half-wave rectifier which outputs the positive threshold value according to the positive values of the input signal; and

   first reset means which is enabled according to the negative peak value fed back from the negative peak value detector (350), and which resets the positive threshold value to the predetermined value.

5. The peak detector of claim 4, wherein the first reset means comprises a first transistor (Q1) having a base connected to the output of the negative peak value detector via a base resistor (R1), a collector connected to the output of the first half-wave rectifier, and an emitter connected to a predetermined reference voltage source (Vr), to reset the positive threshold value output from the first half-wave rectifier to a reference voltage of the reference voltage source according to the active state of the negative peak value.

6. The peak detector of claim 2, 3, 4 or 5 wherein the second automatic threshold controller (340) comprises:

   a second half-wave rectifier which outputs the negative threshold value according to the negative values of the input signal; and

   second reset means which is enabled according to the positive peak value fed back from the positive peak value detector (330), and resets the negative threshold value to the predetermined value.

7. The peak detector of claim 6, wherein the second reset means comprises a second transistor (Q2) having a base connected to the output of the positive peak value detector via a base resistor (R2), a collector connected to the output of the second half-wave rectifier, and an emitter connected to a prede-

termined reference voltage source (Vr), to reset the negative threshold value output from the second half-wave rectifier to a reference voltage of the reference voltage source according to the active state of the positive peak value.

8. The peak detector of any of claims 2 to 7, further comprising a plurality of amplifiers which separate the input signal into two signals each having positive and negative values, and amplify the separated signals to output to the first and second automatic threshold controllers (320, 340), respectively.

9. A data detector for a digital recording/reproducing apparatus including an equalizer (302) which equalizes a reproduced signal and outputs an equalized signal, a peak detector (304) which detects positive and negative peak values of the equalized signal according to positive and negative threshold values, for respectively detecting the positive and negative peak values, and a Viterbi decoder (305) which receives the positive and negative peak values for a Viterbi decoding, the data detector comprising:

a positive peak value detector (330) which compares an input signal having digital information with the positive threshold value to detect the positive peak value;

a negative peak value detector (350) which compares the input signal with the negative threshold value to detect the negative peak value;

a first automatic threshold controller (320) which controls the positive threshold value according to the input signal having a positive value, to reset the positive threshold value to a predetermined value based on the negative peak value; and

a second automatic threshold controller (340) which controls the negative threshold value according to the input signal having a negative value, to reset the negative peak value to a predetermined value based on the positive peak value.

10. The data detector of claim 9, wherein the predetermined value of the first automatic threshold controller (320) and the predetermined value of the second automatic threshold controller (340) are the same as each other.

11. The data detector of claim 9, wherein the first automatic threshold controller (320) comprises:

a first half-wave rectifier which outputs the positive threshold value according to the positive values of the input signal; and

first switching means which is enabled according to the negative peak value fed back from the negative peak value detector, and sets the positive threshold value to the predetermined value.

12. The data detector of claim 11, wherein the first switching means comprises a first transistor (Q1) having a base connected to the output of the negative peak value detector via a base resistor (R1), a collector connected to the output of the first half-wave rectifier, and an emitter connected to a predetermined reference voltage source, to set the positive threshold value output from the first half-wave rectifier to the reference voltage of the reference voltage source according to the active state of the negative peak value.

13. The data detector of claim 9 10, 11 or 12, wherein the second automatic threshold controller (340) comprises:

a second half-wave rectifier which outputs the negative threshold value according to the negative values of the input signal; and

second switching means which is enabled according to the positive peak value fed back from the positive peak value detector, and which sets the negative threshold value to the predetermined value.

14. The data detector of claim 13, wherein the second switching means comprises a second transistor (Q2) having a base connected to the output of the positive peak value detector via a base resistor (R2), a collector connected to the output of the second half-wave rectifier, and an emitter connected to a predetermined reference voltage source, to set the negative threshold value output from the second half-wave rectifier to the reference voltage of the reference voltage source according to the active state of the positive peak value.

15. The data detector of claim 9, further comprising a plurality of amplifiers which separate the input signal into two signals each having positive and negative values, and amplify the separated signals to output to the first and second automatic threshold controllers, respectively.

16. A peak detection method comprising the steps of:

(a) detecting (330, 350) positive and negative

peak values from an input signal having digital information, based on positive and negative threshold values; and

(b) detecting (320, 340) each threshold value according to positive and negative values of the input signal, to reset each threshold value to a predetermined value based on the detected peak value having the opposite polarity thereto.

17. A peak detection method for improving performance of Viterbi decoding in a maximum likelihood system, the method comprising the steps of:

(a) comparing (330) an input signal having digital information with a positive threshold value for detecting a positive peak value, to detect the positive peak value;

(b) comparing (350) the input signal with a negative threshold value for detecting a negative peak value, to detect the negative peak value;

(c) detecting (320) the positive threshold value according to the positive values of the input signal and resetting the positive threshold value to a predetermined value based on the negative peak value; and

(d) detecting (340) the negative threshold value according to the negative values of the input signal and resetting the negative threshold value to a predetermined value based on the positive peak value.

18. The peak detection method of claim 17, wherein the predetermined value of the step (c) and the predetermined value of the step (d) are the same as each other.

FIG. 1

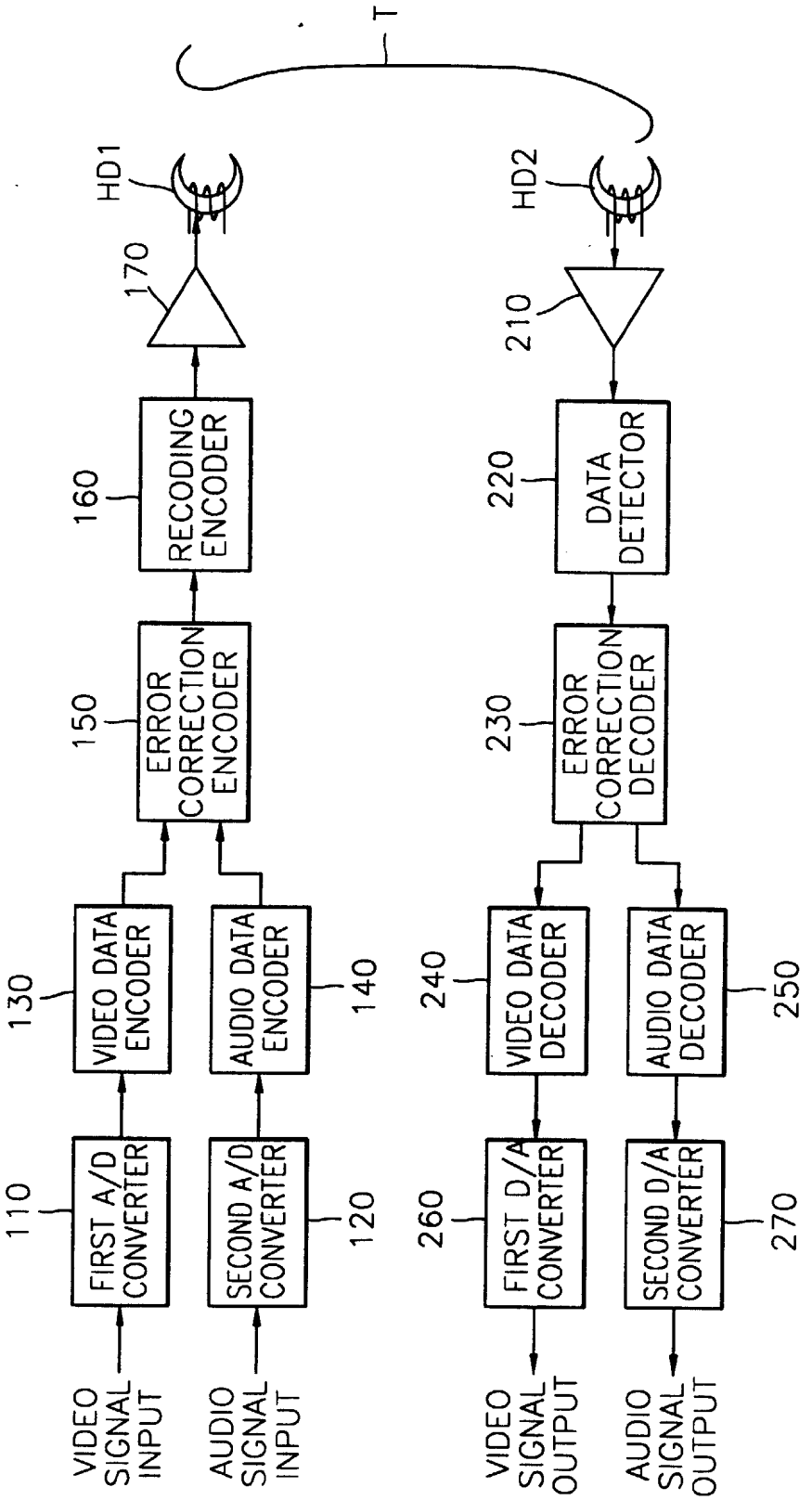

T
HD1
HD2
170
210
160
RECODING ENCODER
220
DATA DETECTOR
150
ERROR CORRECTION ENCODER
230
ERROR CORRECTION DECODER
130
VIDEO DATA ENCODER
140
AUDIO DATA ENCODER
240
VIDEO DATA DECODER
250
AUDIO DATA DECODER
110
FIRST A/D CONVERTER
120
SECOND A/D CONVERTER
260
FIRST D/A CONVERTER
270
SECOND D/A CONVERTER
VIDEO SIGNAL INPUT
AUDIO SIGNAL INPUT
VIDEO SIGNAL OUTPUT
AUDIO SIGNAL OUTPUT

FIG. 2 (PRIOR ART)

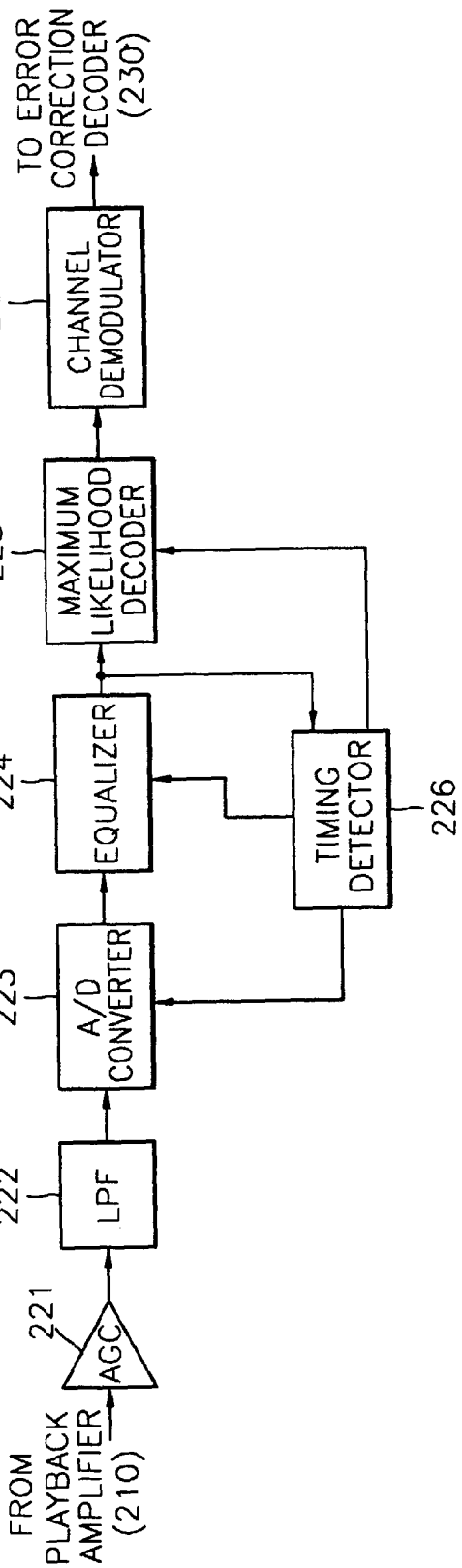


FIG. 3

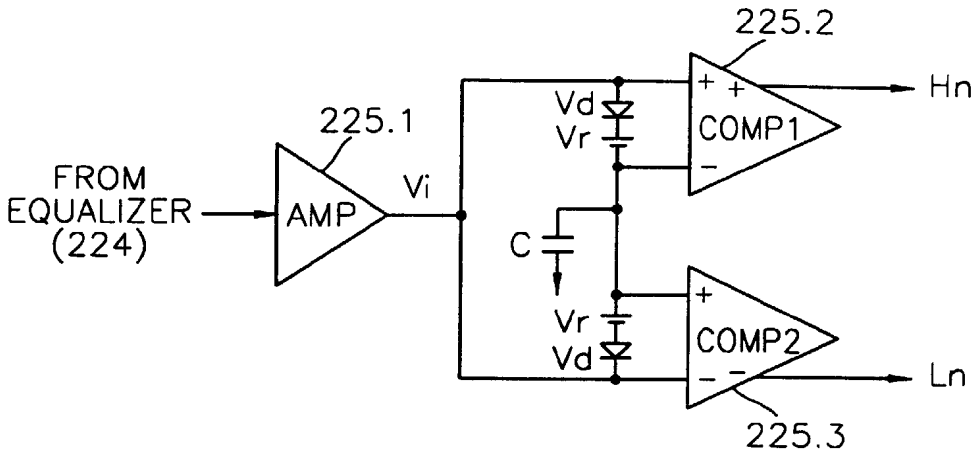

225.2
Hn
Vd
Vr
COMP1
225.1
FROM
EQUALIZER
(224)
AMP
Vi
C
Vr
Vd
COMP2
Ln
225.3

FIG. 4

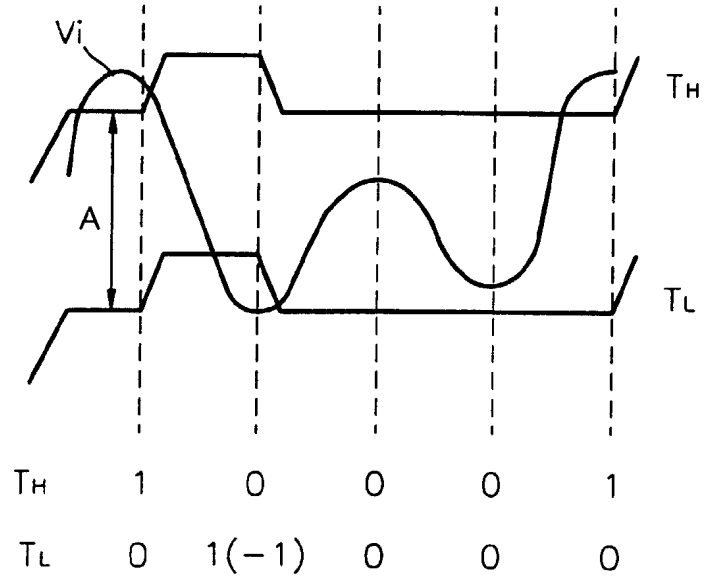

Vi
TH
A
TL
TH 1 0 0 0 1
TL 0 1(−1) 0 0 0

FIG. 5

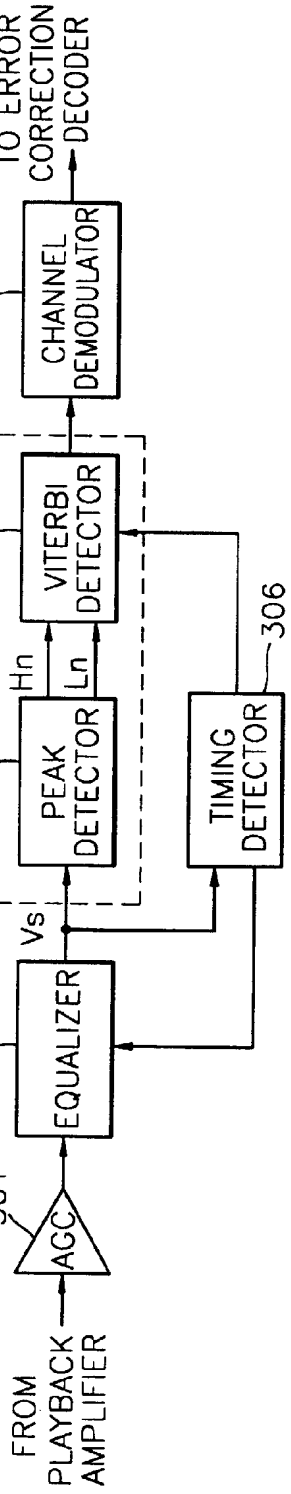

FROM PLAYBACK AMPLIFIER
301
AGC
302
EQUALIZER
Vs
303
304
PEAK DETECTOR
Hn
Ln
305
VITERBI DETECTOR
306
TIMING DETECTOR
307
CHANNEL DEMODULATOR
TO ERROR CORRECTION DECODER

FIG. 6

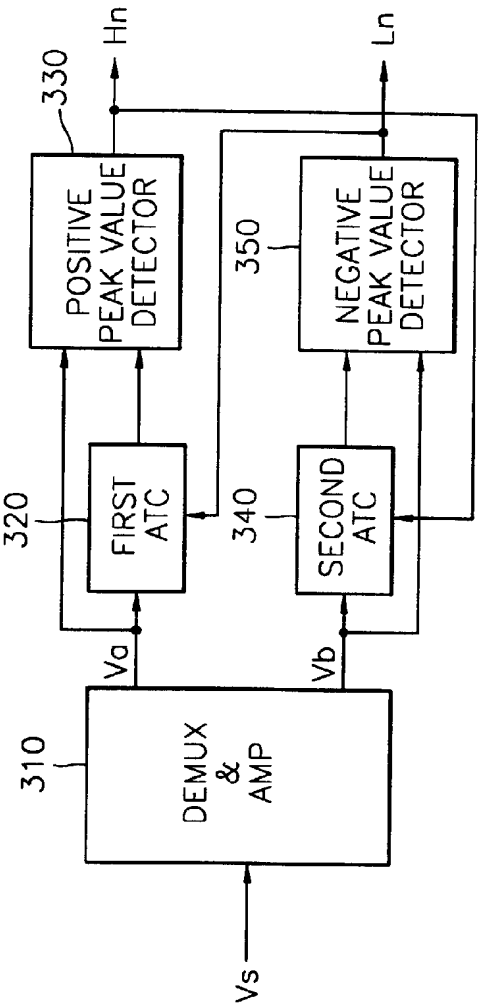

Vs
310
DEMUX & AMP
Va
Vb
320
FIRST ATC
340
SECOND ATC
330
POSITIVE PEAK VALUE DETECTOR
350
NEGATIVE PEAK VALUE DETECTOR
Hn
Ln

FIG. 7

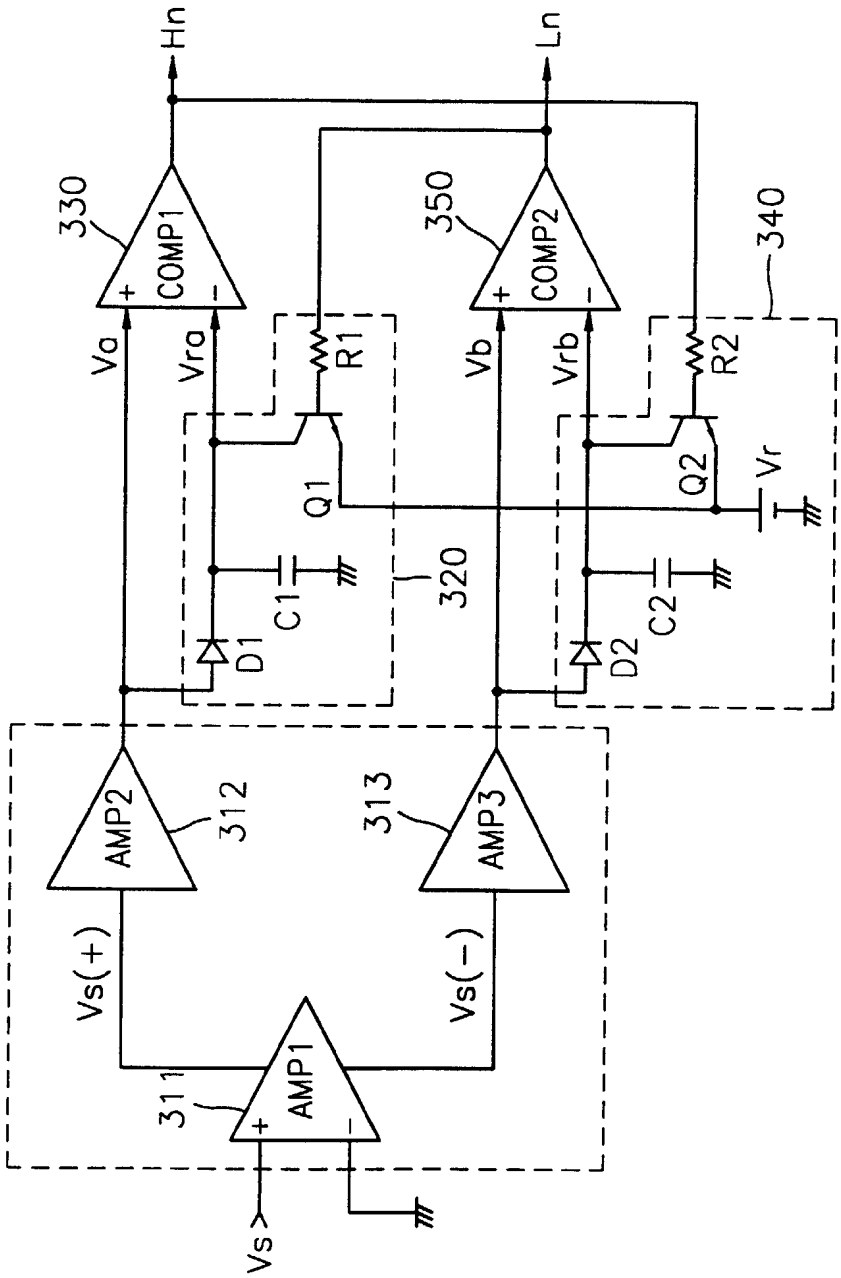

Hn
Ln
330
COMP1
350
COMP2
340
Va
Vra
R1
Vb
Vrb
R2
Q1
Q2
Vr
C1
320
C2
D1
D2
312
AMP2
313
AMP3
Vs(+)
Vs(-)
311
AMP1
Vs

FIG. 8A

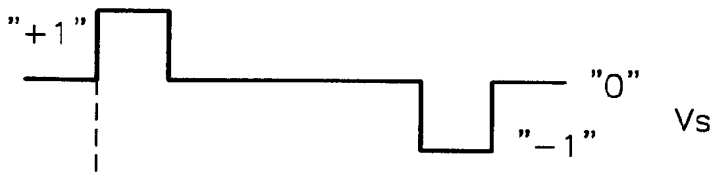


FIG. 8B

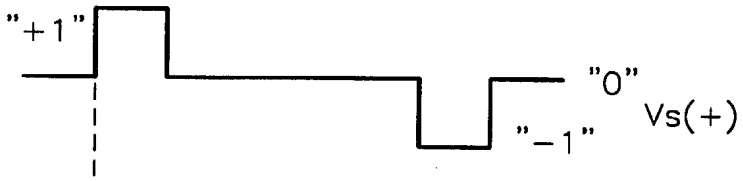


FIG. 8C

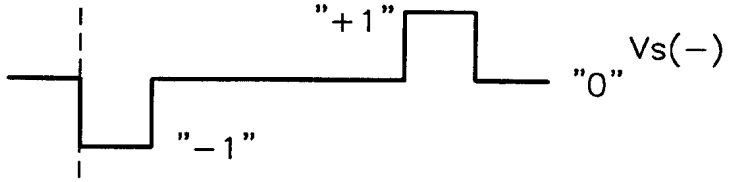


FIG. 8D

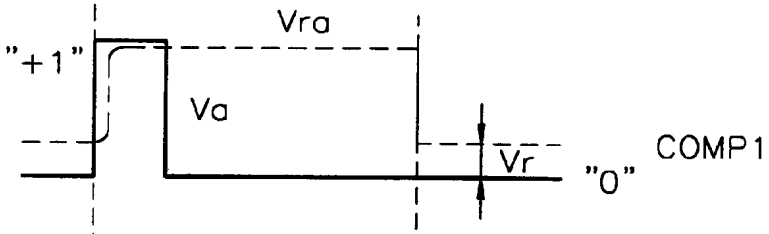


FIG. 8E

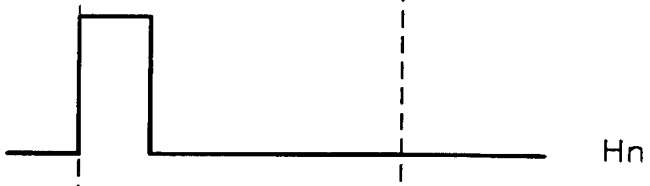


FIG. 8F

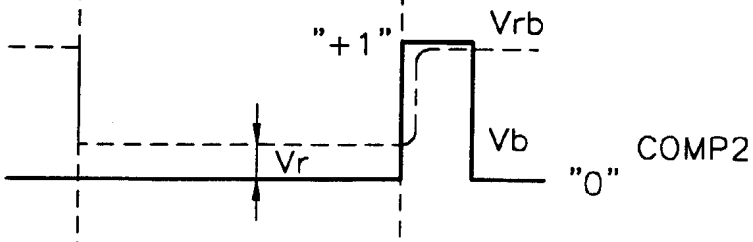
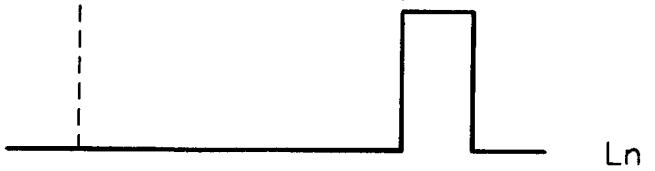


FIG. 8G



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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 0377

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 371 400 A (DEUTSCH FRANZ FORSCH INST) 6 June 1990 * column 4, line 32 - column 6, line 23; figure 3 *	1-4,6, 16-18	H03K5/1532 G11B20/10 H03K5/08
Y		8	
A		9-15	

Y	EP 0 551 858 A (SAMSUNG ELECTRONICS CO LTD) 21 July 1993 * figure 2 *	8	

A	BOLOGNESI G ET AL: "ANALOG SWITCH CUTS PEAK-DETECTOR RESET TIME" EDN ELECTRICAL DESIGN NEWS, vol. 40, no. 11, 25 May 1995, page 88 XP000520332 * the whole document *	5,7	

A	MARGUERRE, HANS: "Der goldene Mittelweg" ELEKTRONIK, vol. 33, no. 9, May 1989, pages 65-68, XP002082042 München, DE		TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K G01R G11B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 October 1998	Jepsen, J

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